Abstract of the disclosure

Is disclosed a flash memory device that includes a control circuit for generating a count-up pulse signal notifying a generation of an address required for a burst read operation. An address generator circuit generates an address in response to the count-up pulse signal, and a discharge circuit discharges global bit lines in response to the count-up pulse signal. According to this control scheme, the global bit lines may be discharged before the local and global bit lines are selected.